What is claimed is:

1   1.   An apparatus comprising:

2   a storage structure to store at least one entry, the at least one entry to include a register

3   identifier value;

4   a first physical rename register of a first length; and

5   a second physical rename register of a second length different than the first length;

6   wherein the register identifier value is to indicate a current length, wherein the current

7   length is selected from a set including the first length and the second length.

1   2.   The apparatus of claim 1, wherein:

2   the first and second rename registers belong to a plurality of n physical rename registers,

3   wherein n > 2;

4   each of the n physical rename registers is of a distinct length; and

5   the set includes each of the n distinct lengths.

1   3.   The apparatus of claim 1, wherein:

2   the storage structure is to store a plurality of entries, each of the plurality of entries to

3   include a corresponding register identifier value.

1   4.   The apparatus of claim 1, wherein:

2   the first physical rename register is one of a plurality (z) of physical rename registers of

3   the first length.

1 5.   The apparatus of claim 1, wherein:

2   the second physical rename register is one of a plurality (m) of physical rename registers

3   of the second length.

1 6.   The apparatus of claim 4, wherein:

2   the second physical rename register is one of a plurality (m) of physical rename registers

3   of the second length.

1 7.   The apparatus of claim 6, wherein:

2   z is not equal to m.

1 8.   The apparatus of claim 1, further comprising:

2   a logical register; and

3   rename logic to map an instance of the logical register to a selected physical rename

4   register, where the selected physical rename register is selected from a plurality of registers

5   comprising the first physical rename register and the second physical rename register.

1   9.   The apparatus of claim 8, wherein:

2   the logical register includes a plurality of n bit positions;

3   a selected one of the n bit positions may be accessed individually responsive to a first

4   instruction that indicates the selected bit position;

5   all n bit positions may be accessed together responsive to a second instruction; and

6   the rename logic is further to allocate the first physical rename register responsive to the

7   first instruction, the rename logic further to allocate the second physical rename register

8   responsive to the second instruction.

1   10.   The apparatus of claim 9, wherein:

2   a subset including y of the n bits may be accessed responsive to a third instruction, where

3   y > 1; and

4   the rename logic is further to allocate the first physical rename register responsive to the

5   third instruction.

1   11.   The apparatus of claim 10, wherein:

2   the length of the first physical rename register includes y bit positions.

1   12.   The apparatus of claim 11, wherein:

2   the entry is further to include a position identifier, the position identifier to indicate a

3   selected one of the y bit positions of the first physical rename register.

1   13.   The apparatus of claim 12, wherein:

2   the selected one of the y bit positions of the first physical rename register corresponds to

3   the selected bit position indicated by the first instruction.

1   14.   A method comprising:

2   determining if a current instruction indicates a multiple-bit-field (MBF) register having n

3   bit positions, where $n > 1$;

4   wherein the MBF register is to be written in accordance with any of a plurality of access

5   types, the plurality of access types including:

6   a partial-bit write of 1 bit position;

7   a bulk-bit write of x bit positions, where $1 < x \leq n$;

8   allocating a physical rename register for the destination register;

9   wherein allocating further comprises allocating a physical rename register of a first length

10   if the current instruction indicates a partial-bit write and further comprises allocating a

11   physical rename register of a second length if the current instruction indicates a bulk-bit

12   write.

1   15.   The method of claim 14, wherein:

2   allocating further comprises modifying a rename map table to indicate the allocated

3   physical rename register.

1   16.   The method of claim 14, wherein:

2   the plurality of access types further includes a partial-bit write of y bit positions, where 1

3        $< y < x$.

1   17.   The method of claim 14, wherein:

2   the y bit positions are contiguous.

1   18.   The method of claim 14, wherein:

2   the x bit positions are contiguous.

1   19.   The method of claim 14, wherein:

2   the plurality of access types includes a bulk-bit write of all n bit positions.

1   20.   The method of claim 16, wherein:

2   y=2.

1   21.   The method of claim 16, wherein:

2   y=4.

1   22.   The method of claim 14, further comprising:

2   modifying the current instruction to indicate the allocated physical rename register in place of the

3   MBF register.